UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,723	01/03/2002	Gregory C. Desalvo	AFD 459	2134

26902 7590 07/30/2003

DEPARTMENT OF THE AIR FORCE
AFMC LO/JAZ
2240 B ST., RM. 100
WRIGHT-PATTERSON AFB, OH 45433-7109

EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,723	DESALVO ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/21/2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *10-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 22-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's cancellation to claims 10-21 is acknowledged. Claims 31-37 are newly added. Thus, claims 1-9 and 22-37 are pending in this application.

Election/Restrictions

2. Applicant's election without traverse of claims 1-9 and 22-30 in Paper No. 4 is acknowledged.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In reference to claim 26, applicants recite, "...wherein said desirable high frequency electrical characteristics include thin substrate-determined electrical parameters within said integrated circuit device...". This renders the claim indefinite, since it fails to further limit the invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-9, 31-35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morcom et al. (U.S. 6,162,702) in view of Uchiyama et al. (U.S. 2003/003724 A1).

In reference to claims 1, 31, 33, 34 and 37, Morcom et al. (1A-6) in a related method to form ultra thin silicon wafers teach disposing a grid pattern (4, 5) on the backside of a silicon wafer (2) comprising silicon; said grid pattern mask (4, 5) including a backside periphery outline masking for each circuit die of said wafer (2); and removing a layer (1) of selected thickness form said wafer backside surface, wherein said removing being from exposed backside surface areas intermediate elements of said grid pattern masking (4, 5), wherein said removing step leaving recessed valley portions of selected thickness disposed intermediate individual circuit die-strengthening upstanding (3) surrounding bluff masked semiconductor regions in said wafer backside surface (column 2, line 15 – column 3, line 45).

Morcom et al. fail to expressly teach forming an array of via holes of selected location and depth dimension in said wafer of circuit die; said step of forming an array of via holes being performed during a front side accessing of said wafer of circuit die; metallizing said via hole openings, said metallizing including establishing via metal electrical connections with selected of said contact pads; and disposing the mask pattern on the back side of a microwave radio frequency die. However, Uchiyama et al. (Figs.3a-3g and Figs.6a-6f) in a related method to form microwave radio frequency integrated circuit dies teach forming an array of via holes (13) of selected location and depth dimension in a wafer (10) of circuit die, wherein said step of forming an array of

via holes (13) being performed during a front side accessing of said wafer (10) of circuit die; and disposing a mask pattern on the back side of said microwave radio frequency die ([0060] – [0064] and [0086] – [0095]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchiyama et al. and Morcom et al. to enable forming the circuit configuration of Uchiyama et al. in the wafer of Morcom et al. to arrive at the claimed invention, and furthermore, because this will result in a microwave radio frequency circuit die with improved high frequency, dissipating heat generated during operation (Uchiyama et al., [0002] – [0008]), while using the physical integrity of the silicon wafer to provide reinforcement to the thin wafer (Morcom et al., column 1, lines 21 – 31).

In reference to claim 2, the combined teachings of Morcom et al. and Uchiyama et al. substantially teach wherein said wafer has an initial thickness between five hundred and six hundred twenty five micrometers and has a final thickness of between twenty five and one hundred micrometers in said removed layer recessed valley portions (Morcom et al., column 3, lines 7 – 18).

In reference to claim 3, the combined teachings of Morcom et al. and Uchiyama et al. teach wherein said step of forming an array of via holes is performed after fabrication of said microwave radio frequency circuit on said die (Uchiyama et al., [0060] – [0064]).

In reference to claim 4, the combined teachings of Morcom et al. and Uchiyama et al. substantially teach all aspects of the invention by fail to show forming an etching step vernier marker pattern in each die backside surface of said wafer after said step of

forming an array of front side via hole. However, portion of the ridges in Morcom et al. (see Fig.6) could perform the function required of by recitation of "vernier markers", which is a label or statement of intended use.

In reference to claim 5, the combined teachings of Morcom et al. and Uchiyama et al. teach wherein said backside periphery outline masking is disposed in a closed geometric pattern encircling each front side microwave radio frequency circuit die and further include a closed geometric backside annular ring of original wafer thickness semiconductor material surrounding said entire wafer of microwave radio frequency circuit die (Morcom et al., column 2, line 53 – column 3, line 6).

In reference to claims 6-8 and 35, the combined teachings of Morcom et al. and Uchiyama et al. teach wherein said step of removing selected thickness from said wafer backside surface etching step comprises a backside etching sequence (Morcom et al., column 2, lines 23 – 33); wherein said backside surface etching step comprises a dry gas etching step (Morcom et al., column 2, lines 23 – 33); and wherein said backside surface etching step includes one of an inductively coupled plasma and an electron cyclotron resonance fast etching processes (Uchiyama et al., [0048] and [0063]).

In reference to claim 9, the combined teachings of Morcom et al. and Uchiyama et al. teach wherein said removing step individual circuit die-strengthening upstanding surrounding bluff masked regions further include a wafer periphery-surrounding annular ring upstanding bluff region (Morcom et al., Fig.6).

In reference to claim 32, the combined teachings of Morcom et al. and Uchiyama et al. teach wherein said array of circuit die locations and circuit die segregation

boundaries defined across a frontal surface of said semiconductor wafer and said upstanding mesa array of original wafer thickness extent across said backside surface each comprise a rectangular grid pattern (Morcom et al., Fig.6).

7. Claims 22-30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morcom et al. ('702) in view of Uchiyama et al. ('724 A1) and Suzuki et al. (U.S. 2003/0119281).

In reference to claims 22, 26 and 36, Morcom et al. (1A-6) in a related method to form ultra thin silicon wafers teach depositing a mask (4, 5) of grid pattern-defining configuration on wafer (2) backside surface; said mask (4, 5) of grid pattern-defining configuration determining a plurality of wafer (2) backside grid cells each aligned in surrounding periphery with one of said wafer (2) frontal surface integrated circuit devices; removing a controlled thickness (1) amount of semiconductor wafer (2) backside surface semiconductor material within each said backside grid cell, said removing including an etching step and leaving a wafer (2) backside grid pattern of semiconductor material of said semiconductor wafer (2) nominal thickness dimension and leaving a selected thickness remainder amount of said semiconductor wafer (2) nominal thickness dimension material, within each said backside grid cell, supporting said integrated circuit device; said etching step also leaving a wafer perimeter-disposed backside ring (3) of wafer semiconductor material of said semiconductor wafer (2) nominal thickness dimension and integral interconnection with said wafer backside grid pattern of wafer nominal thickness dimension; said wafer perimeter-disposed backside ring of wafer semiconductor material of said semiconductor wafer nominal thickness

dimension and said wafer backside grid pattern of wafer nominal thickness dimension semiconductor material in interconnecting combination adding physical handling-assisting substantial physical integrity and rigidity to said now thinned semiconductor wafer (column 2, line 15 – column 3, line 45).

Morcom et al. fail to expressly teach fabricating electrical circuit portions of said thinned semiconductor wafer radio frequency integrated circuit device on a frontal side of a nominal thickness semiconductor wafer, each said integrated circuit device being disposed in a separate die location of said semiconductor wafer and including a plurality of contact pads; forming a plurality of via hole intrusions into said nominal thickness semiconductor wafer in locations registered with selected of said contact pads of said integrated circuit device; said via hole intrusions being formed from said frontal side of said nominal thickness semiconductor wafer metallizing said via hole openings, said metallizing including establishing via metal electrical connections with selected of said contact pads; and covering said thinned semiconductor wafer backside including said wafer backside grid pattern cells with a layer of ground plane metal, said covering including forming ground plane electrical interconnections with said via hole intrusions metallization; mounting said wafer on said frontal surface thereof.

However, Uchiyama et al. (Figs.3a-3g, Figs.6a-6f and Fig.7) in a related method to form microwave radio frequency integrated circuit dies teach fabricating electrical circuit portions of said thinned semiconductor wafer radio frequency integrated circuit device on a frontal side of a nominal thickness semiconductor wafer (10), each said integrated circuit device being disposed in a separate die location of said semiconductor

wafer and including a plurality of contact pads (59); forming a plurality of via hole intrusions (13) into said nominal thickness semiconductor wafer (10) in locations registered with selected of said contact pads (59) of said integrated circuit device; said via hole intrusions (13) being formed from said frontal side of said nominal thickness semiconductor wafer; metallizing said via hole openings (13), said metallizing including establishing via metal electrical connections with selected of said contact pads (59); thinning said semiconductor wafer (10); and covering said thinned semiconductor wafer backside including said wafer backside grid pattern cells with a layer of ground plane metal (14), said covering including forming ground plane electrical interconnections with said via hole intrusions metallization; and mounting said wafer (10) on said frontal surface thereof (column 2, line 15 – column 3, line 45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchiyama et al. and Morcom et al. to enable forming the circuit configuration of Uchiyama et al. in the wafer of Morcom et al. to arrive at the claimed invention, and furthermore, because this will result in a microwave radio frequency circuit die with improved high frequency, dissipating heat generated during operation (Uchiyama et al., [0002] – [0008]), while using the physical integrity of the silicon wafer to provide reinforcement to the thin wafer (Morcom et al., column 1, lines 21 – 31).

The combined teachings of Morcom et al. and Uchiyama et al. fail to teach further processing said wafer during continued frontal surface mounting, said further processing including removing each integrated circuit device die from said wafer by wafer segregation within a lateral extent of a backside grid cell. However, Suzuki et al.

(Figs.1A-6) in a related method to form thinned wafers for the fabrication of microwave radio frequency devices teach processing a wafer (1) during a continued frontal surface mounting, said further processing including removing each integrated circuit device die (15) from said wafer (1) by wafer segregation within a lateral extent of a backside grid cell ([0040] – [0043]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Suzuki et al. with the teachings of Morcom et al. and Uchiyama et al. to enable the die separation to complete the processing of the semiconductor die.

In reference to claim 23, the combined teachings of Morcom et al. Uchiyama et al. and Suzuki et al. teach wherein said step of forming a plurality of via hole intrusions into said semiconductor wafer includes disposing said via hole intrusions to a first depth dimension into said semiconductor wafer; and wherein said selected thickness remainder amount of said semiconductor wafer nominal thickness dimension material in said step of removing a controlled thickness amount of said wafer backside semiconductor material within each said backside grid cell comprises leaving a selected thickness remainder amount of said wafer nominal thickness equal to said via, hole intrusions first depth dimension into said semiconductor wafer (Morcom et al., column 2, line 53 – column 3, line 6 and Uchiyama et al., Figs.3a-3g).

In reference to claim 24, the combined teachings of Morcom et al., Uchiyama et al. and Suzuki et al. teach wherein said semiconductor wafer of nominal thickness is between five hundred and six hundred twenty-five micrometers in thickness; and wherein said selected thickness remainder amount of said wafer nominal thickness and

said via hole intrusions first depth dimension are each no more than one hundred micrometers (Morcom et al., column 3, lines 7 – 18).

In reference to claim 25 the combined teachings of Morcom et al., Uchiyama et al. and Suzuki et al. teach wherein said radio frequency integrated circuit device is comprised of one of field effect and bipolar junction and heterojunction bipolar transistors (Uchiyama et al., [0023]).

In reference to claim 27 the combined teachings of Morcom et al., Uchiyama et al. and Suzuki et al. teach wherein said depositing step mask is a metallic mask (Uchiyama et al., [0016]).

In reference to claims 28 and 29, the combined teachings of Morcom et al., Uchiyama et al. and Suzuki et al. teach wherein said etching removing step comprises a dry gas etching step (Morcom et al., column 2, lines 23 – 33); and wherein etching removing step includes one of an inductively coupled plasma and an electron cyclotron resonance fast etching processes (Uchiyama et al., [0048] and [0063]).

In reference to claim 30, the combined teachings of Morcom et al., Uchiyama et al. and Suzuki et al. teach wherein said covering step forming of ground plane electrical interconnections comprises covering underside portions of etching-exposed second smaller diameter via hole metallizations with ground plane metal (Uchiyama et al., [0062] and Suzuki et al., [0043]).

Conclusion

8. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823

Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
7/22/03

George Fourson
Primary Examiner